## REMARKS

Claims 1-10, 13-18, 20-22, 24 and 25 remain pending in the instant application. Claims 1-10, 13-18, 20-22, 24 and 25 presently stand rejected. Claims 1, 2, 14, 15, 21, 24, and 25 are amended herein. No new matter has been added. Entry of this amendment and reconsideration of the pending claims are respectfully requested.

*Claim Rejections – 35 U.S.C. § 103*

Claims 1, 7-9, 14-17, 20-22, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Banerjee (US 6,820,127 B2) in view of Brustoloni et al. (US 6,625,149 B1) and Ganfield (US 2004/0218631).

Claims 2-6, 10, 13, 18, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Banerjee in view of Brustoloni et al. and Ganfield as applied to claims 1, 8, 14, and 25 above, and further in view of Kaniyar et al (US 7,219,121).

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

Claim 1 as previously presented recites:

> A method comprising: receiving a packet at a network device**; pre-fetching a protocol control block (PCB) associated with the received packet into a cache of a selected processing unit**; queuing the received packet for processing; pre-fetching a header associated with the received packet into the cache of the

selected processing unit; and **retrieving the PCB for the received packet from the cache of the selected processing unit when the selected processing unit is ready to process the received packet**.

In contrast, the combined references do not teach or suggest (at least) the above-emphasized portion of the claim. The Office Action alleges (in page 2) that Banerjee teaches pre-fetching a protocol control block (PCB) associated with the [received] packet into a cache of a selected processing unit. For example, the Office Action recites step 502 (7:25-30) and step 522 (8:1-6) of Fig. 5 in support of this assertion. Step 522 is recited as copying the PCB associated with a socket into the PCB cache. Thus, the Office Action asserts that copying the PCB into a PCB cache is "pre-fetching."

Applicants traverse this assertion because Banerjee teaches processing the PCB **before** the PCB is copied into the PCB cache. Banerjee teaches steps 516 and 517 for doing connection processing that must be executed before copying the PCB into the PCB cache. Furthermore, when the PCB is found to be in the cache (steps 508 and 510), the processing is performed without writing the PCB into the PCB cache. Thus, the PCB for the received packet is not "pre-fetched" because connection processing for the packet is **processed before** the PCB is copied into a cache. Figure 4, step 414 is inapposite because step 414 applies to creation of a socket for a connection (step 402) and does not teach or fairly suggest receiving a packet (which, for example, an associated PCB is pre-fetched) as recited by the instant claim.

The Office Action cites steps 504, 508, 512, and 513 (7:30-42) as teaching retrieving the PCB from the cache when a processing unit is ready to process the packet. As discussed above, this is not pre-fetching because the PCB of Banerjee is read **from** a

cache to be [immediately] processed, and is not, for example, pre-fetched into a cache for later processing. Furthermore Banerjee fails to teach or fairly suggest retrieving the PCB for the received packet from the cache of the selected processing unit when the selected processing unit is ready to process the received packet. Instead, Banerjee teaches retrieving a stored PCB when a **subsequent** packet is encountered. In other words, Banerjee teaches retrieving a PCB that was stored when a **previous** packet was encountered. Accordingly, Banerjee fails to teach or fairly suggest retrieving the PCB for the received packet from the cache of the selected processing unit when the selected processing unit is ready to process the received packet.

The Office Action admits that Banerjee fails to expressly disclose queuing the received packet for processing. The Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's method and article by incorporating the step of queuing the received packets for processing as allegedly taught by Brustoloni. Brustoloni fails to overcome the deficiencies of Banerjee because Brustoloni does not teach or fairly suggest **pre-fetching a protocol control block (PCB) associated with the received packet into a cache of a selected processing unit** and **retrieving the PCB for the received packet from the cache of the selected processing unit when the selected processing unit is ready to process the received packet** as discussed above.

The Office Action admits that Banerjee fails to expressly disclose pre-fetching a header associated with the packet into the cache of the selected processing unit. The Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's method and article by

incorporating a step for comprising pre-fetching a header associated with the packet in a cache, as allegedly taught by Ganfield. Instead, Ganfield (paragraphs 38 and 39) storing a length (L) from a PCB in a buffer descriptor cache in header information 526. Thus the information being stored is not the packet header (see dependent claim 3 of the instant application), and is instead derived from the PCB. Thus Ganfield fails to overcome the deficiencies of Brustoloni and Banerjee, either singly or in motivated combination. Accordingly claim 1 is believed to be allowable.

.

Claim 14, as amended, recites:

14. (Currently Amended) An article of manufacture comprising: a machine accessible medium including content that when accessed by a machine causes the machine to: receive a packet; pre-fetch a protocol control block (PCB) associated with the packet and a packet header of the packet into a cache of a processing unit; queue the packet for processing; retrieve the PCB from the cache when the processing unit is ready to process the packet; and to pre-fetch a PCB for a packet to be sent when the to-be-sent packet is queued for transmission across a network wherein the PCB for the to-be-sent packet is pre-fetched in response to a send request being initiated for the to-be-sent packet.

In addition to the reasons stated above with respect to claim 1, claim 14 is also believed to be allowable because the cited art fails to teach or suggest the above emphasized limitations. For example, Banerjee fails to pre-fetch a PCB for a to-be-sent packet for transmission across a network. Instead, for example, Banerjee teaches (Fig. 7,

step 718) delivery to an appropriate user process. Thus claim 14 is believed to be allowable. Claim 21 is believed to be allowable for at least reasons stated above.

Dependent claims are at least allowable for the reasons by which the claims from which they depend are allowable. Moreover, with respect to claim 2, the cited references fail to teach wherein the PCB is pre-fetched in response to receiving the received packet before processing the received packet. As discuss above, Banerjee processes the received packet **before** caching a PCB for the received packet. Also as discussed above, the cached PCB is retrieved at a later time for another packet. The cited references, singly or in fairly motivated combination thus fail to teach or fairly suggest the limitations of claim 2, which is allowable. Applicants request that the instant §103(a) rejections of the claims be withdrawn.

## CONCLUSION

In view of the foregoing amendments and remarks, it is believed that the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

## CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: June 11, 2008

/Mark Hennings/

Mark R. Hennings
Reg. No. 48,982

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
Phone (206) 292-8600

**CERTIFICATE OF MAILING/TRANSMISSION**

I hereby certify that this correspondence is being transmitted electronically via EFS-Web to the United States Patent and Trademark Office on the date shown below.

/Elizabeth J. Martinez/ June 11, 2008
Elizabeth J. Martinez ***Date***